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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/693,074	10/23/2003	Nhon Quach	42390.P7442C	2223

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Chui-Kiu Teresa Wong
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025-1026

EXAMINER	
ROJAS, MIDYS	
ART UNIT	**PAPER NUMBER**
2185	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/11/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/693,074	QUACH ET AL.	
	Examiner	Art Unit	
	Midys Rojas	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The indicated allowability of claim 5 is withdrawn in view of the Morioka reference. Rejections based on Morioka et al. (6,631,447) follow.

Response to Arguments

1. Applicant's arguments with respect to claims 1-5 have been considered but are not persuasive.

Applicant argues that the area limit attribute information of Morioka et al. is not a property of the operating system. However, Morioka discloses that for every access from any processor, there is provided area limit attribute information to be retained in its translation lookaside buffer (Col. 5, lines 1-27). Since the accesses of the processor are governed by the instructions of an operating system, the limit are attribute is dependent on the operating system's control of the access request and can therefore, be considered to be a property of the operating system. Additionally, the area limit attribute information is held in the translation lookaside buffer (Col. 4, lines 61-67) which is controlled by the functions of the operating system (Col. 14, lines 48-64), therefore, the area limit attribute information is under the control of the operating system and is therefore considered to be a property of the operating system.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Morioka et al. (6,631,447).

Regarding Claim 1, Morioka discloses a processor [Fig. 1, 100] comprising:

a translation-lookaside-buffer (TLB) [Col. 4, lines 47-67, "processors, each having... a translation lookaside buffer..."];

a cache to provide temporary storage for a data block ["processors, each having a cache memory..."]; and

a memory management unit ["cache coherency control"] to implement a first cache-coherency mechanism [cache coherency only for cache memories in one of said plurality of clusters] or a second cache-coherency mechanism [or for every one of the cache memories through the system] using the TLB according to a property of an operating system to be run by the processor [using the limit attribute information being held in the TLB and in response to an access request from any one of the processors].

Morioka discloses that for every access from any processor, there is provided area limit attribute information to be retained in its translation lookaside buffer (Col. 5, lines 1-27). Since the accesses of the processor are governed by the instructions of an operating system, the limit are attribute is dependent on the operating system's control of the access request and can therefore, be considered to be a property of the operating system. Additionally, the area limit attribute information is held in the translation lookaside buffer (Col. 4, lines 61-67) which is

controlled by the functions of the operating system (Col. 14, lines 48-64), therefore, the area limit attribute information is under the control of the operating system and is therefore considered to be a property of the operating system.

Regarding Claim 2, Morioka discloses the processor wherein the TLB includes a plurality of entries, each entry including a virtual address tag, a physical address [translates virtual addresses into real addresses, therefore it must include a plurality of virtual and physical addresses], and a memory attribute [holds area attribute information, see Col. 5, lines 28-46].

Regarding Claim 3, Morioka discloses the processor wherein the first cache coherency mechanism [cache coherency issued within a local cluster] snoops the cache if an access to a memory address designated by an uncacheable memory attribute is detected [the transaction issued within the local cluster is snooped by the local bus cache coherency control, Col. 23, line 65- Col. 24, line 5].

Regarding Claim 4, Morioka discloses a computer system [Fig. 1] comprising:

an execution core [processor];

a cache having a plurality of data entries [processor comprises an instruction cache memory and a data cache memory, Col. 5, lines 28-46];

a memory to store an operating system for the computer system [instructions stored in main memory]; and

a memory management unit [cache coherency control, Col. 4, lines 47-67] to manage data flow among the execution core, the cache and the memory, the memory management unit to operate in a first cache coherency mode [cache coherency only for cache memories in one of said plurality of clusters] or a second cache coherency mode [or for every one of the cache memories

through the system] according to a property of the operating system [using the limit attribute information being held in the TLB and in response to an access request from any one of the processors].

Morioka discloses that for every access from any processor, there is provided area limit attribute information to be retained in its translation lookaside buffer (Col. 5, lines 1-27). Since the accesses of the processor are governed by the instructions of an operating system, the limit are attribute is dependent on the operating system's control of the access request and can therefore, be considered to be a property of the operating system. Additionally, the area limit attribute information is held in the translation lookaside buffer (Col. 4, lines 61-67) which is controlled by the functions of the operating system (Col. 14, lines 48-64), therefore, the area limit attribute information is under the control of the operating system and is therefore considered to be a property of the operating system.

Claim 5 is rejected using the same rationale as that of Claim 4 wherein there is no evidence that Morioka's second cache coherency mode supports memory attribute aliasing (operate in a first cache coherency mode **or** a second cache coherency mode...).

Claim 6 is rejected using the same rationale as that of Claim 4.

Regarding Claim 7, Morioka discloses the method wherein booting the computer system in the first cache coherency mode [cache coherency issued within a local cluster] comprises configuring a memory management unit to self-snoop a cache in response to selected memory accesses [the transaction issued within the local cluster is snooped by the local bus cache coherency control, Col. 23, line 65- Col. 24, line 5].

Regarding Claim 8, Morioka discloses the method wherein booting the computer system in the second cache coherency mode comprises configuring a memory management unit to forward selected memory accesses to a cache to detect memory attribute conflicts [compares a physical address portion and a comparison tag portion in a comparator and sends the result to the bus cache coherency control, when there is a hit, a dirty bit is selected, Col. 24, lines 7-21].

Regarding Claims 9-10, Morioka discloses the method wherein the first cache coherency mode supports memory attribute aliasing and the second cache coherency mode does not support memory attribute aliasing. The method of the invention operates in a first cache coherency mode **or** a second cache coherency mode, and the second cache coherency mode does not support memory attribute aliasing. There is no evidence that Morioka's second cache coherency mode supports memory attribute aliasing.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Midys Rojas whose telephone number is (571) 272-4207. The examiner can normally be reached on M-F 5:30am - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571) 272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

January 5, 2007

Midys Rojas
Examiner
Art Unit 2185

MR

SANJIV SHAH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

SANJIV SHAH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100